CLAIMS

I/We claim:

1. A method of manufacturing a microelectronic component probe card, comprising:

forming a plurality of blind holes that extend inwardly from a front face of a substrate, each hole having a closed bottom spaced from a back face of the substrate by a back thickness;

filling each of the holes with an electrically conductive metal, the metal in each hole defining a conductor;

removing the back thickness of the substrate, exposing tips of the conductors; and

selectively removing a further thickness of the substrate to define an array of pins extending outwardly from a remaining thickness of the substrate, each pin comprising an exposed length of one of the conductors.

2. The method of claim 1 wherein the array of pins is arranged to mate with an array of contacts carried by a microelectronic component.

3. The method of claim 1 wherein each hole has a diameter of about 10-60 microns.

4. The method of claim 1 wherein each hole has a diameter of at least about 60 microns.

5. The method of claim 1 wherein each hole has a diameter of about 60-200 microns.

6. The method of claim 1 wherein each pin extends at least about 20 microns beyond a back surface of the reduced thickness substrate.

7. The method of claim 1 wherein each pin extends about 20-200 microns beyond a back surface of the reduced thickness substrate.

8. The method of claim 1 wherein removing the back thickness of the substrate comprises abrading the back face of the substrate with an abrasive medium.

9. The method of claim 1 wherein removing the further thickness of the substrate comprises selectively etching the substrate.

10. The method of claim 1 wherein removing the further thickness of the substrate comprises removing the entire thickness of the substrate.

11. The method of claim 10 further comprising joining the substrate to a backing member after filling the holes and prior to removing the further thickness of the substrate.

12. The method of claim 1 further comprising joining the substrate to a flexible backing member after filling the holes and prior to removing the further thickness of the substrate, removing the further thickness of the substrate comprising removing the entire thickness of the substrate.

13. The method of claim 1 further comprising depositing an intermediate layer on an internal surface of the hole before filling the hole with the metal.

14. The method of claim 1 further comprising depositing an intermediate layer of a non-metallic material on an internal surface of the hole before filling the hole with the metal.

15. The method of claim 1 wherein an excess of the metal is deposited on the substrate when filling the via, the excess comprising an overburden on the front face of the substrate.

16. The method of claim 15 further comprising removing at least a portion of the overburden to electrically isolate the conductors from one another.

17. The method of claim 15 further comprising removing the overburden by polishing to electrically isolate the conductors from one another.

18. The method of claim 15 further comprising selectively removing a patterned portion of the overburden to electrically isolate the conductors from one another.

19. The method of claim 15 further comprising removing at least a portion of the overburden to expose a portion of the front face of the substrate and applying a fill layer on the exposed front face of the substrate.

20. The method of claim 19 further comprising attaching a confronting face of a backing member to the fill layer, the backing member being electrically coupled to each of the pins.

21. The method of claim 1 further comprising depositing an electrical contact material on a surface of each of the conductors proximate the front face of the substrate.

22. The method of claim 1 further comprising juxtaposing a confronting face of a backing member with the front face of the substrate and joining the backing member and the substrate.

23. The method of claim 1 further comprising electrically coupling the conductors to a backing member.

24. The method of claim 1 further comprising dividing the substrate into a series of cards, each card including a thickness of the substrate and a plurality of the pins.

25. The method of claim 1 wherein the array of pins is arranged to mate with an array of contacts carried by a microelectronic component.

26. A method of manufacturing a microelectronic component probe card, comprising:

forming a blind hole that extends inwardly from a front face of a substrate, the hole having a closed bottom spaced from a back face of the substrate by a back thickness;

substantially filling the hole with a conductive material;

removing the back thickness of the substrate, exposing a tip of the conductive material; and

removing a further thickness of the substrate to expose a length of the conductive material having a surface adapted to establish temporary electrical contact with a contact on a microelectronic component.

27. The method of claim 26 wherein the hole has a diameter of about 10-60 microns.

28. The method of claim 26 wherein the hole has a diameter of at least about 60 microns.

29. The method of claim 26 wherein the hole has a diameter of about 60-200 microns.

30. The method of claim 26 wherein the exposed length of the conductive material extends at least about 20 microns beyond a back surface of the reduced thickness substrate.

31. The method of claim 26 wherein the exposed length of the conductive material extends about 20-200 microns beyond a back surface of the reduced thickness substrate.

32. The method of claim 26 wherein removing the back thickness of the substrate comprises abrading the back face of the substrate with an abrasive medium.

33. The method of claim 26 wherein removing the further thickness of the substrate comprises selectively etching the substrate.

34. The method of claim 26 wherein filling the hole with the conductive material comprises depositing a metal in the hole by a process selected from the group consisting of CVD, PVD, electroless deposition, and electroplating.

35. The method of claim 26 further comprising depositing an intermediate layer on an internal surface of the hole before filling the hole with the conductive material.

36. The method of claim 26 further comprising depositing an intermediate layer on an internal surface of the hole before filling the hole with the conductive material, the intermediate layer being formed a material which is different from the conductive material.

37. The method of claim 36 wherein the conductive material comprises a conductive metal, the method further comprising depositing an intermediate layer of a non-metallic material on an internal surface of the hole before filling the hole with the conductive metal.

38. The method of claim 26 wherein an excess of the conductive material is deposited on the substrate when filling the via, the excess comprising an overburden on the front face of the substrate.

39. The method of claim 38 wherein the conductive material in the hole comprises a conductor, the method further comprising removing at least a portion of the overburden to electrically isolate the conductor.

40. The method of claim 38 wherein the conductive material in the hole comprises a conductor, the method further comprising removing the overburden by polishing to electrically isolate the conductor.

41. The method of claim 38 wherein the conductive material in the hole comprises a conductor, the method further comprising selectively removing a patterned portion of the overburden to electrically isolate the conductor.

42. The method of claim 38 wherein the conductive material in the hole comprises a conductor, the method further comprising removing at least a portion of the overburden to expose a portion of the front face of the

substrate and applying a fill layer on the exposed front face of the substrate.

43. The method of claim 38 wherein the conductive material in the hole comprises a conductor, the method further comprising removing at least a portion of the overburden to electrically isolate the conductor and depositing an electrical contact material on a surface of the conductor proximate the front face of the substrate.

44. The method of claim 26 wherein the conductive material in the hole comprises a conductor, the method further comprising depositing an electrical contact material on a surface of the conductor proximate the front face of the substrate.

45. The method of claim 26 further comprising juxtaposing a confronting face of a backing member with the front face of the substrate and joining the backing member and the substrate.

46. The method of claim 26 wherein the conductive material in the hole comprises a conductor, the method further comprising electrically coupling the conductor to a backing member.

47. A method of manufacture, comprising:

forming an array of blind holes that extend inwardly from a front face of a substrate, each hole having a closed bottom spaced by a back thickness from a back face of the substrate;

depositing an intermediate layer on an internal surface of at least some of the holes;

depositing an electrically conductive metal on the substrate, the metal filling each of the holes and defining an overburden on the front face, the metal in each hole defining a conductor;

removing at least a portion of the overburden to electrically isolate each of the conductors from one another;

removing a portion of the substrate including the back thickness to define an array of pins extending outwardly from a remaining thickness of the substrate, each pin comprising an exposed length of one of the conductors;

joining a backing member with the substrate and electrically coupling the array of pins to contacts carried by the backing member.

48. The method of claim 47 wherein the joined backing member and substrate comprise a composite member, further comprising dividing the composite member into a series of probe cards, each probe card including a thickness of the composite member and a plurality of the pins.

49. The method of claim 47 further comprising electrically connecting the backing member to a test system.

50. The method of claim 47 further comprising temporarily contacting the array of pins to a mating array of contacts carried by a microelectronic component.

51. The method of claim 50 further comprising delivering a test signal to the microelectronic component with at least one of the pins.

52. A microelectronic component testing system, comprising:

a substrate having a front face, a back face, and a plurality of openings extending from the front face to the back face in an array;

an intermediate layer on an inner surface of each opening;

an array of electrically isolated conductors patterned from an integral metal layer, each conductor having a contact end adjacent the front surface of the substrate, an intermediate length received in one of the openings in the substrate, and an exposed length extending outwardly beyond the back surface of the substrate a distance of no more than 200 microns; and

a backing member joined to the substrate and having a confronting surface oriented toward the substrate front surface, the confronting surface carrying a plurality of electrical contacts, each of which is electrically coupled to the contact end of one of the conductors.

53. The microelectronic component testing system of claim 52 wherein the substrate comprises undoped silicon.

54. The microelectronic component testing system of claim 52 wherein each of the conductors has a diameter no greater than 200 microns.

55. The microelectronic component testing system of claim 52 wherein each of the conductors has a diameter no greater than 60 microns.

56. The microelectronic component testing system of claim 52 wherein each of the conductors has a diameter of about 10-60 microns.

57. The microelectronic component testing system of claim 52 wherein the backing member comprises a flexible tape.

58. The microelectronic component testing system of claim 52 wherein the backing member comprises a printed circuit board.

59. The microelectronic component testing system of claim 52 further comprising a controller and a power supply, the controller being operatively connected to the backing member to monitor test performance of a microelectronic component.